19-5541; Rev 1; 3/11

Octal High-Voltage Transmit/Receive Switches

General Description

The MAX4936–MAX4939 are octal, high-voltage, transmit/receive (T/R) switches. The T/R switches are based on a diode bridge topology, and the amount of current in the diode bridges can be programmed through an SPI™ interface. All devices feature a latch-clear input to asynchronously turn off all T/R switches and put the device into a low-power shutdown mode. The MAX4936/MAX4938 include the T/R switch and grass-clipping diodes, performing both transmit and receive operations. The MAX4937/MAX4939 include just the T/R switch and perform the receive operation only.

The MAX4936/MAX4938 transmit path is low impedance during high-voltage transmit and high impedance during low-voltage receive, providing isolation between transmit and receive circuitry. The high-voltage transmit path is high bandwidth, low distortion, and low jitter.

The receive path for all devices is low impedance during low-voltage receive and high impedance during high-voltage transmit, providing protection to the receive circuitry. The low-voltage receive path is high bandwidth, low noise, low distortion, and low jitter. Each T/R switch can be individually programmed on or off, allowing these devices to also be used as receive path multiplexers.

The MAX4936/MAX4937 feature clamping diodes to protect the receiver input from voltage spikes due to leakage currents flowing through the T/R switches during transmission. The MAX4938/MAX4939 do not have clamping diodes and rely on clamping diodes integrated in the receiver front end.

All devices are available in a small, 56-pin, 5mm x 11mm TQFN package, and are specified over the commercial 0°C to +70°C temperature range.

Features

- ♦ **Low Power: Low Impedance (5Ω) with 1.5mA Bias Current Only**
- ♦ **Low Noise < 0.5nV/$\sqrt{\text{Hz}}$ (typ) with 1.5mA Bias Current Only**
- ♦ **Wide -3dB Bandwidth 65MHz (typ)**
- ♦ **Easy Programming with SPI Interface**
- ♦ **High Density (8 Channels per Package)**
- ♦ **Grass-Clipping Diodes with Low-Voltage Isolation (MAX4936/MAX4938)**
- ♦ **Output Clamp Diodes for Receiver Protection (MAX4936/MAX4937)**
- ♦ **Global Shutdown Control (CLR)**
- ♦ **Each T/R Switch Can Be Individually Programmed On or Off**
- ♦ **Low-Voltage Receive Path with High-Voltage Protection**
- ♦ **Space-Saving, 5mm x 11mm, 56-Pin TQFN Package**

Applications

Medical/Industrial Imaging

Ultrasound

High-Voltage Transmit and Low-Voltage Isolation

Ordering Information/Selector Guide

PART	LOW-VOLTAGE ISOLATION	HIGH-VOLTAGE PROTECTION	OUTPUT CLAMP	TEMP RANGE	PIN-PACKAGE
MAX4936CTN+	Yes	Yes	Yes	0°C to +70°C	56 TQFN-EP*
MAX4937CTN+	No	Yes	Yes	0°C to +70°C	56 TQFN-EP*
MAX4938CTN+**	Yes	Yes	No	0°C to +70°C	56 TQFN-EP*
MAX4939CTN+**	No	Yes	No	0°C to +70°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Future product—contact factory for availability.*

Octal High-Voltage Transmit/Receive Switches

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{DD} Positive Supply Voltage..................................-0.3V to +6V
V_{CC}, LVCC_ Positive Supply Voltage ....-0.3V to +6V
V_{EE}, LVEE_ Negative Supply Voltage ....-6V to +0.3V
CLK, DIN, CLR, $\overline{LE}$ Input Voltage ....-0.3V to +6V
DOUT Output Voltage ....-0.3V to (V_{DD} + 0.3V)
HV_ Input Voltage (MAX4936/MAX4938) ....-120V to +120V
COM_ Input/Output Voltage...............................-120V to +120V
NO_ Output Voltage (MAX4936/MAX4937) .... ±1.5V
NO_ Output Voltage (MAX4938/MAX4939) .... ±6V
Voltage Difference Across Any or
All HV_ (MAX4936/MAX4938) .... ±230V
Voltage Difference Across Any or All COM_ .... ±230V
Continuous Current (HV_ to COM_) (MAX4936/MAX4938)..±250mA
Continuous Current (Any Other Terminal)..................... ±100mA
Peak Current (HV_ to COM_) (MAX4936/MAX4938)
(Pulsed at 1ms, 0.1% Duty Cycle) .... ±2.5A
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 41.0mW/°C above +70°C) 3279mW
Operating Temperature Range............................. 0°C to +70°C
Storage Temperature Range............................ -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...........44°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).................10°C/W

Note 1: Package thermal resistance were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.7V to +5.5V, V_{EE} = -2.7V to -5.5V, V_{CLR} = 0V, LVCC_ = V_{CC}, LVEE_ = V_{EE}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS						
HV_ Input Voltage Range	$V_{IRHV\_}$	MAX4936/MAX4938 only	-115		+115	V
|Difference Across Any or All HV_ |		MAX4936/MAX4938 only			220	V
COM_ Output Voltage Range	$V_{ORCM\_}$	$\|V_{HV\_}\| \geq$ +2V, $I_{HV\_}$ = ±100mA (MAX4936/MAX4938 only)	$V_{HV\_}$ - 1	$V_{HV\_}$ ± 0.85	$V_{HV\_}$ + 1	V
COM_ Input Voltage Range	$V_{IRCM\_}$		-115		+115	V
|Difference Across Any or All COM_ |					220	V
NO_ Output Voltage Range	$V_{ORNO\_}$	V_{CC} = +5V, V_{EE} = -5V, $\|V_{COM\_}\| \geq$ +2V, R_L = 200Ω, C_L = 30pF, $I_{CH\_}$ = 10mA (MAX4936/MAX4937 only)	-1	±0.75	+1	V
		V_{CC} = +5V, V_{EE} = -5V, $\|V_{COM\_}\| \leq$ +0.4V, R_L = 200Ω, C_L = 30pF, $I_{CH\_}$ = 1.5mA	$V_{COM\_}$ - 0.2	$V_{COM\_}$ ± 0.1	$V_{COM\_}$ + 0.2	
HV_ to COM_ Continuous Current	$I_{CN\_}$	$V_{COM\_}$ = 0V (MAX4936/MAX4938 only)	-200		+200	mA
HV_ to COM_ Drop	$V_{CN\_}$	$V_{COM\_}$ = 0V, $I_{CN\_}$ = ±2A (MAX4936/MAX4938 only)		±2		V
Diode Bridge Voltage Offset	$V_{OFF\_}$	V_{CC} = +5V, V_{EE} = -5V, COM_ = unconnected, NO_ = unconnected, I_{CH} = 1.5mA	-200		+200	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.7V to +5.5V, V_{EE} = -2.7V to -5.5V, V_{CLR} = 0V, LVCC_ = V_{CC}, LVEE_ = V_{EE}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
HV_ Off-Leakage Current	$I_{LHV\_}$	$\|V_{HV\_} - V_{COM\_}\| \le$ +0.3V, $V_{COM\_}$ = 0V (MAX4936/MAX4938 only)		-3		+3	µA
COM_ Off-Leakage Current	$I_{LCOM\_}$	$\|V_{HV\_} - V_{COM\_}\| \le$ +0.3V, $V_{HV\_}$ = 0V, switch is off (MAX4936/MAX4938 only)		-3		+3	µA
		HV_ = unconnected, switch is off (MAX4936/MAX4938 only)		-1		+1	µA
		Switch is off (MAX4937/MAX4939 only)		-1		+1	µA
NO_ Off-Leakage Current	$I_{LNO\_}$	$\|V_{NO\_}\| \le$ +0.3V, switch is off	MAX4936/MAX4937	-2		+2	µA
			MAX4938/MAX4939	-1		+1	
DYNAMIC CHARACTERISTICS							
Diode Bridge Turn-On Time	t_{ON}	V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, I_{CH} = 1.5mA, C_L = 30pF, $V_{COM\_}$ = ±0.4V, Figure 1				200	ns
Diode Bridge Turn-Off Time	t_{OFF}	V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, I_{CH} = 1.5mA, C_L = 30pF, $V_{COM\_}$ = ±0.4V, Figure 1				5	µs
Reverse Recovery Time	t_{RR}	I_{FWD} = I_{RVR} = 10mA			450		ns
SPI Power-Up Delay	t_{DLY}					500	µs
Small-Signal COM_ to NO_ On Impedance	$R_{ICOM\_}$	V_{CC} = +5V, V_{EE} = -5V, $V_{NO\_}$ = 0V, I_{CH} = 1.5mA, f = 5MHz			4.5		Ω
-3dB Bandwidth	BW	COM_ to NO_, switch is on, $\|V_{COM\_}\| \le$ +0.4V, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA			65		MHz
Off-Isolation	V_{ISO}	HV_ to COM_, $\|V_{HV\_} - V_{COM\_}\| \le$ +0.3V, V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 100pF, f = 1MHz (MAX4936/MAX4938 only)			-50		dB
		COM_ to NO_, switch is off, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, f = 1MHz			-75		
Crosstalk	V_{CT}	Between any two HV_ to COM_ channels, $\|V_{HV\_}\| \ge$ +2V, V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 100pF, f = 5MHz (MAX4936/MAX4938 only)			-60		dB
		Between any two COM_ to NO_ channels, switch is on, $\|V_{COM\_}\| \le$ +0.4V, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 5MHz			-71		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.7V to +5.5V, V_{EE} = -2.7V to -5.5V, V_{CLR} = 0V, LVCC_ = V_{CC}, LVEE_ = V_{EE}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
2nd Harmonic Distortion	HD2	HV_ to COM_, $\lvert V_{COM\_}\rvert \geq$ +2V, V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 100pF, f = 5MHz (MAX4936/MAX4938 only)		-90		dBc
		COM_ to NO_, switch is on, $\lvert V_{COM\_}\rvert \leq$ +0.4V, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 5MHz		-95		
3rd Harmonic Distortion	HD3	HV_ to COM_, $\lvert V_{COM\_}\rvert \geq$ +2V, V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, C_L = 100pF, f = 5MHz (MAX4936/MAX4938 only)		-90		dBc
		COM_ to NO_, switch is on, $\lvert V_{COM\_}\rvert \leq$ +0.4V, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 5MHz		-115		
Two-Tone Intermodulation Distortion (Note 3)	IMD3	COM_ to NO_, switch is on, $\lvert V_{COM\_}\rvert \leq$ +0.4V, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA, f_1 = 5MHz, f_2 = 5.01MHz		-77		dBc
HV_ Off Capacitance	$C_{HV\_(OFF)}$	$\lvert V_{HV\_} - V_{COM\_}\rvert \leq$ +0.3V (MAX4936/MAX4938 only)		12		pF
COM_ Off Capacitance	$C_{COM\_(OFF)}$	$\lvert V_{HV\_} - V_{COM\_}\rvert \leq$ +0.3V, switch is off (MAX4936/MAX4938 only)		17		pF
		Switch is off (MAX4937/MAX4939 only)		12		
NO_ On Capacitance	$C_{NO\_(ON)}$	$\lvert V_{NO\_}\rvert$ < +0.4V, switch is on		20		pF
NO_ Off Capacitance	$C_{NO\_(OFF)}$	$\lvert V_{NO\_}\rvert$ < +0.4V, switch is off		7.5		pF
DIGITAL I/Os (CLR, DIN, DOUT, CLK, $\overline{LE}$)						
Input High Voltage	V_{IH}	V_{DD} = +2.25V to +5.5V	V_{DD} - 0.5			V
		V_{DD} = +1.62V to +1.98V	1.4			
Input Low Voltage	V_{IL}	V_{DD} = +2.25V to +5.5V			0.6	V
		V_{DD} = +1.62V to +1.98V			0.4	
Input Hysteresis	V_{HYST}	V_{DD} = +3V		50		mV
		V_{DD} = +1.8V		90		
Input Leakage Current	I_{IL}	CLR, DIN, CLK, $\overline{LE}$ = GND or V_{DD}	-1		+1	µA
Input Capacitance	C_{IN}			5		pF
DOUT Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
DOUT High Voltage	V_{OH}	I_{SOURCE} = 5mA	V_{DD} - 0.4			V
POWER SUPPLY (V_{DD}, V_{CC}, V_{EE})						
Positive Logic Supply Voltage	V_{DD}		+1.62		+5.5	V
Positive Analog Supply Voltage	V_{CC}		+2.7		+5.5	V
Negative Analog Supply Voltage	V_{EE}		-5.5		-2.7	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +1.62V to +5.5V, V_{CC} = +2.7V to +5.5V, V_{EE} = -2.7V to -5.5V, V_{CLR} = 0V, LVCC_ = V_{CC}, LVEE_ = V_{EE}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Logic Supply Current	I_{DD}	CLR, DIN, CLK, $\overline{LE}$ = GND or V_{DD}			+1	µA
Positive Analog Supply Current	I_{CC}	Per channel, switch is on, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA	+1.15	+1.5	+2	mA
Positive Analog Shutdown Supply Current	I_{CC_SHDN}	CLR = high			+1	µA
Negative Analog Supply Current	I_{EE}	Per channel, switch is on, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA	-2	-1.5	-1.15	mA
Negative Analog Shutdown Supply Current	I_{EE_SHDN}	CLR = high	-1			µA
On Power-Supply Rejection Ratio	$PSRR_{ON}$	V_{CC} to NO_ or V_{EE} to NO_, switch is on, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, I_{CH} = 1.5mA, f = 1MHz		-77		dB
Off Power-Supply Rejection Ratio	$PSRR_{OFF}$	V_{CC} to NO_ or V_{EE} to NO_, switch is off, V_{CC} = +5V, V_{EE} = -5V, R_L = 200Ω, C_L = 30pF, f = 1MHz		-80		dB
LOGIC TIMING (CLR, DIN, DOUT, CLK, $\overline{LE}$) (Figure 1)						
CLK Period	t_{CP}	V_{DD} = 3V ±10%	50			ns
		V_{DD} = 1.8V ±10%	100			
CLK High Time	t_{CH}	V_{DD} = 3V ±10%	20			ns
		V_{DD} = 1.8V ±10%	45			
CLK Low Time	t_{CL}	V_{DD} = 3V ±10%	20			ns
		V_{DD} = 1.8V ±10%	45			
CLK to DOUT Delay	t_{DO}	V_{DD} = 3V ±10%, $C_L \le$ 20pF	3		30	ns
		V_{DD} = 1.8V ±10%, $C_L \le$ 20pF	7		70	
DIN to CLK Setup Time	t_{DS}	V_{DD} = 3V ±10%	10			ns
		V_{DD} = 1.8V ±10%	16			
DIN to CLK Hold Time	t_{DH}	V_{DD} = 3V ±10%	4			ns
		V_{DD} = 1.8V ±10%	4			
CLK to $\overline{LE}$ Setup Time	t_{CS}	V_{DD} = 3V ±10%	36			ns
		V_{DD} = 1.8V ±10%	65			
$\overline{LE}$ Low Pulse Width	t_{WL}	V_{DD} = 3V ±10%	14			ns
		V_{DD} = 1.8V ±10%	22			
CLR High Pulse Width	t_{WC}	V_{DD} = 3V ±10%	20			ns
		V_{DD} = 1.8V ±10%	40			

Note 2: All specifications are 100% production tested at T_A = +70°C, unless otherwise noted. Specifications at 0°C are guaranteed by design.

Note 3: See the *Ultrasound-Specific IMD3 Specification* section.

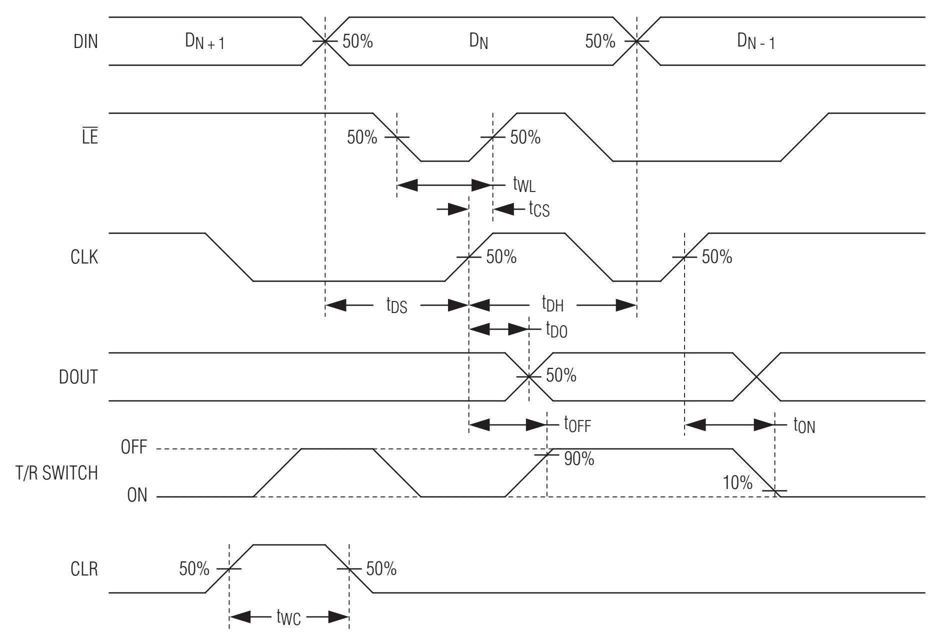
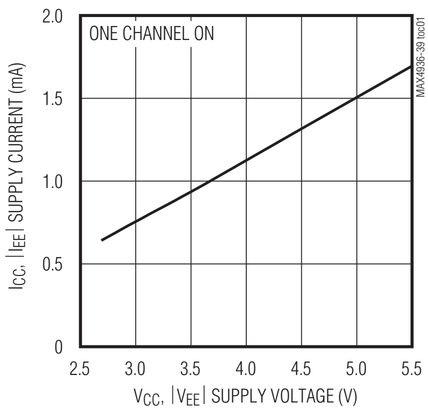


Figure 1. Serial Interface Timing

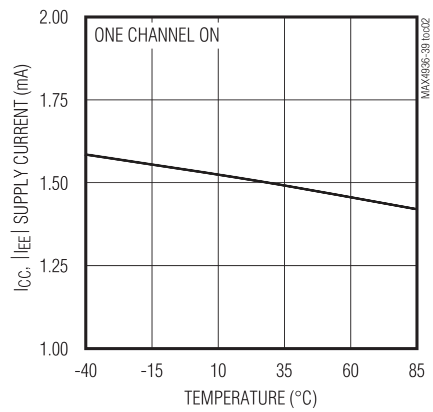
Typical Operating Characteristics

(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA, $R_{COM\_}$ = 200Ω, $R_{NO\_}$ = 200Ω, f = 5MHz, V_{CLR} = 0V, T_A = +25°C, unless otherwise noted.)

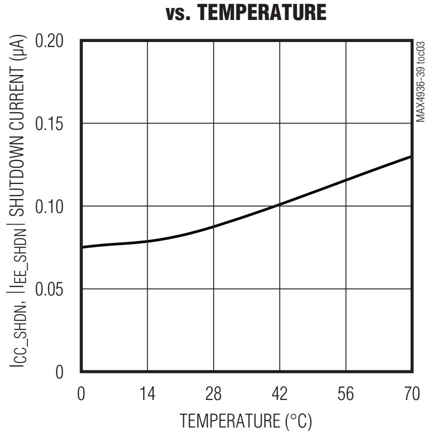
I_{CC}, |I_{EE}| SUPPLY CURRENT vs. V_{CC}, |V_{EE}| SUPPLY VOLTAGE



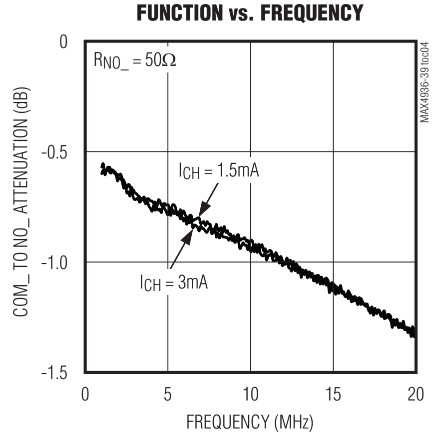
I_{CC}, |I_{EE}| SUPPLY CURRENT vs. TEMPERATURE



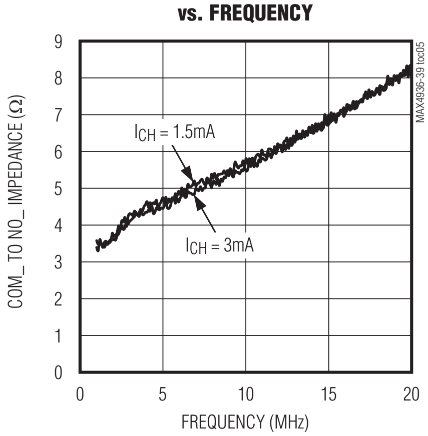
I_{CC_SHDN}, |I_{EE_SHDN}| SUPPLY SHUTDOWN CURRENT vs. TEMPERATURE



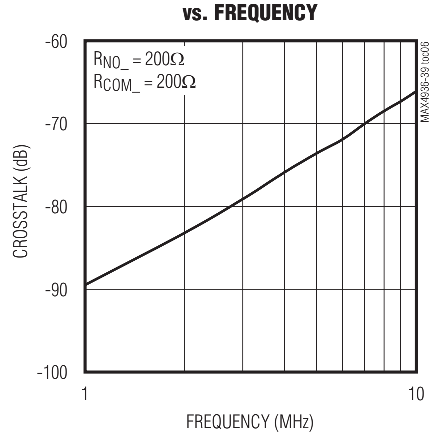
COM_ TO NO_ SMALL-SIGNAL TRANSFER FUNCTION vs. FREQUENCY



COM_ TO NO_ IMPEDANCE vs. FREQUENCY

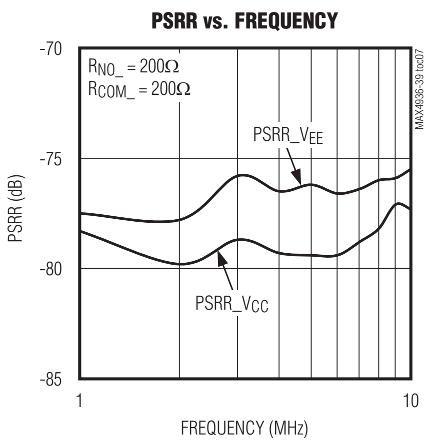


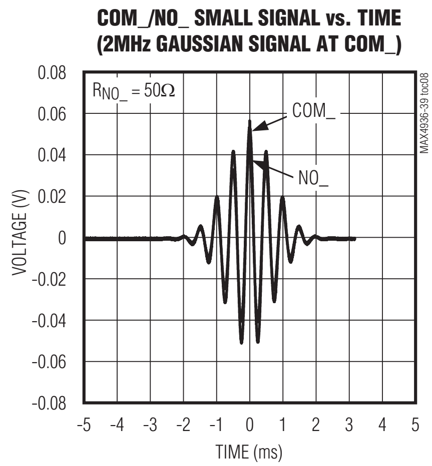
COM_ TO NO_ CROSSTALK vs. FREQUENCY

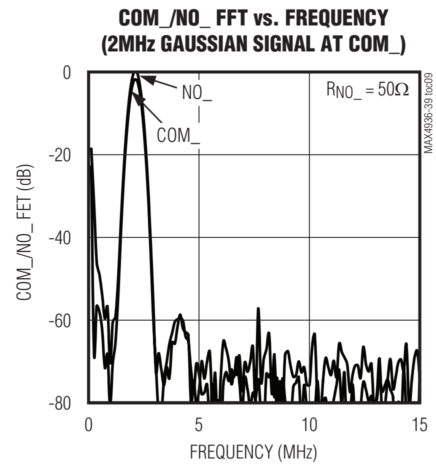


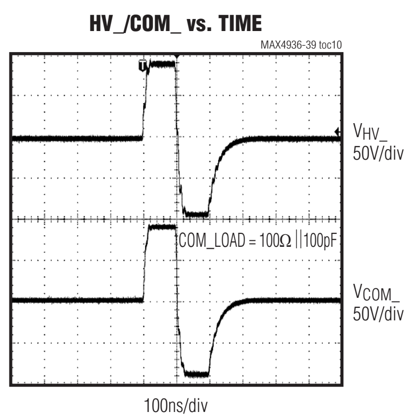
Typical Operating Characteristics (continued)

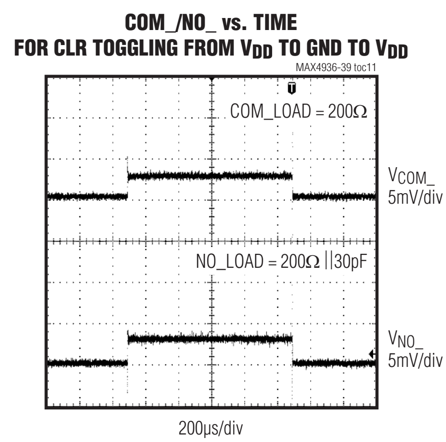
(V_{DD} = +3V, V_{CC} = +5V, V_{EE} = -5V, I_{CH} = 1.5mA, $R_{COM\_}$ = 200Ω, $R_{NO\_}$ = 200Ω, f = 5MHz, V_{CLR} = 0V, T_A = +25°C, unless otherwise noted.)





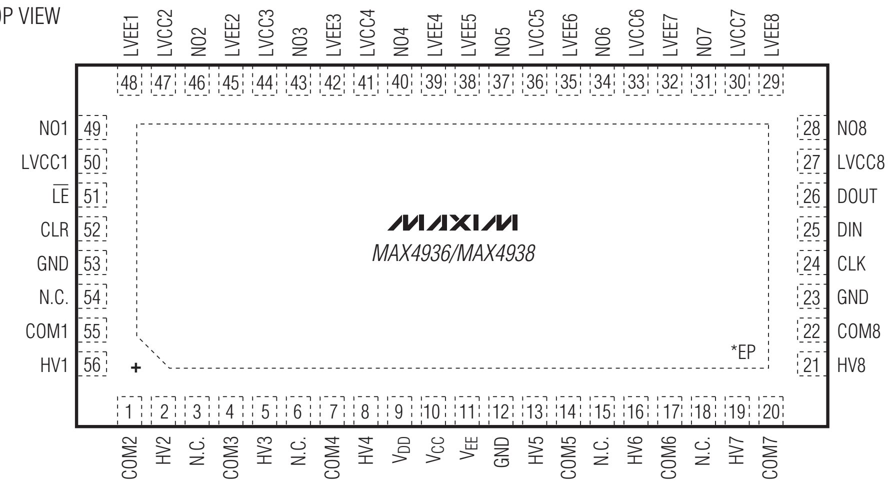


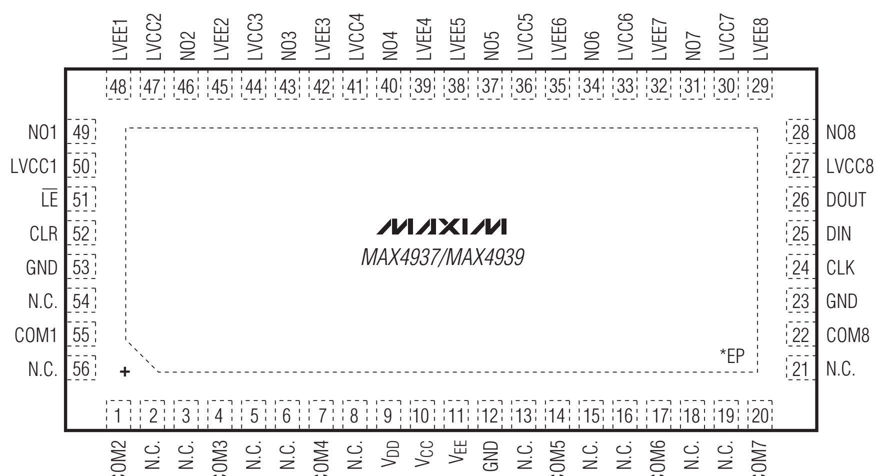




Pin Configuration

TOP VIEW





TQFN
(5mm × 11mm)

*CONNECT EP TO GND.

Pin Description

PIN		NAME	FUNCTION
MAX4936/ MAX4938	MAX4937/ MAX4939		
1	1	COM2	T/R Switch 2 Input. When the switch is on, low-voltage signals are passed through from COM2 to NO2, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
2	—	HV2	T/R Switch 2 Input. COM2 follows HV2 when high-voltage signals are present on HV2. HV2 is isolated from COM2 when low-voltage signals are present on COM2.

Octal High-Voltage Transmit/Receive Switches

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936/ MAX4938	MAX4937/ MAX4939		
3, 6, 15, 18, 54	2, 3, 5, 6, 8, 13, 15, 16, 18, 19, 21, 54, 56	N.C.	No Connection. Not internally connected.
4	4	COM3	T/R Switch 3 Input. When the switch is on, low-voltage signals are passed through from COM3 to NO3, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
5	—	HV3	T/R Switch 3 Input. COM3 follows HV3 when high-voltage signals are present on HV3. HV3 is isolated from COM3 when low-voltage signals are present on COM3.
7	7	COM4	T/R Switch 4 Input. When the switch is on, low-voltage signals are passed through from COM4 to NO4, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
8	—	HV4	T/R Switch 4 Input. COM4 follows HV4 when high-voltage signals are present on HV4. HV4 is isolated from COM4 when low-voltage signals are present on COM4.
9	9	V_{DD}	Positive Logic Supply. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
10	10	V_{CC}	Positive Analog Supply. Bypass V_{CC} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
11	11	V_{EE}	Negative Analog Supply. Bypass V_{EE} to GND with a 1µF or greater ceramic capacitor as close as possible to the device.
12, 23, 53	12, 23, 53	GND	Ground
13	—	HV5	T/R Switch 5 Input. COM5 follows HV5 when high-voltage signals are present on HV5. HV5 is isolated from COM5 when low-voltage signals are present on COM5.
14	14	COM5	T/R Switch 5 Input. When the switch is on, low-voltage signals are passed through from COM5 to NO5, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
16	—	HV6	T/R Switch 6 Input. COM6 follows HV6 when high-voltage signals are present on HV6. HV6 is isolated from COM6 when low-voltage signals are present on COM6.
17	17	COM6	T/R Switch 6 Input. When the switch is on, low-voltage signals are passed through from COM6 to NO6, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
19	—	HV7	T/R Switch 7 Input. COM7 follows HV7 when high-voltage signals are present on HV7. HV7 is isolated from COM7 when low-voltage signals are present on COM7.
20	20	COM7	T/R Switch 7 Input. When the switch is on, low-voltage signals are passed through from COM7 to NO7, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
21	—	HV8	T/R Switch 8 Input. COM8 follows HV8 when high-voltage signals are present on HV8. HV8 is isolated from COM8 when low-voltage signals are present on COM8.
22	22	COM8	T/R Switch 8 Input. When the switch is on, low-voltage signals are passed through from COM8 to NO8, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.

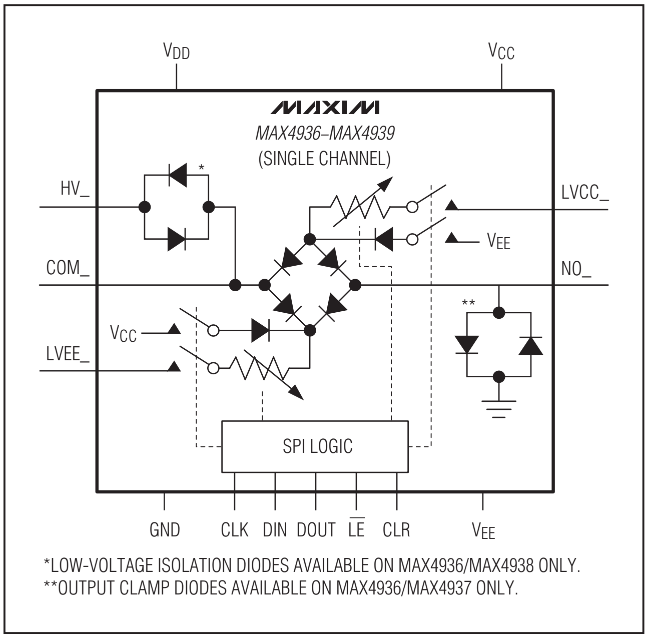
Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936/ MAX4938	MAX4937/ MAX4939		
24	24	CLK	Serial-Clock Input
25	25	DIN	Serial-Data Input
26	26	DOUT	Serial-Data Output
27	27	LVCC8	Inductor V_{CC} Connection. Connect an inductor between LVCC8 and V_{CC} to improve noise performance, otherwise connect LVCC8 to V_{CC}.
28	28	NO8	T/R Switch 8 Output. When the switch is on, low-voltage signals are passed through from COM8 to NO8, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO8 is limited with clamping diodes on MAX4936/MAX4937.
29	29	LVEE8	Inductor V_{EE} Connection. Connect an inductor between LVEE8 and V_{EE} to improve noise performance; otherwise, connect LVEE8 to V_{EE}.
30	30	LVCC7	Inductor V_{CC} Connection. Connect an inductor between LVCC7 and V_{CC} to improve noise performance; otherwise, connect LVCC7 to V_{CC}.
31	31	NO7	T/R Switch 7 Output. When the switch is on, low-voltage signals are passed through from COM7 to NO7, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO7 is limited with clamping diodes on MAX4936/MAX4937.
32	32	LVEE7	Inductor V_{EE} Connection. Connect an inductor between LVEE7 and V_{EE} to improve noise performance; otherwise, connect LVEE7 to V_{EE}.
33	33	LVCC6	Inductor V_{CC} Connection. Connect an inductor between LVCC6 and V_{CC} to improve noise performance; otherwise, connect LVCC6 to V_{CC}.
34	34	NO6	T/R Switch 6 Output. When the switch is on, low-voltage signals are passed through from COM6 to NO6, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO6 is limited with clamping diodes on MAX4936/MAX4937.
35	35	LVEE6	Inductor V_{EE} Connection. Connect an inductor between LVEE6 and V_{EE} to improve noise performance; otherwise, connect LVEE6 to V_{EE}.
36	36	LVCC5	Inductor V_{CC} Connection. Connect an inductor between LVCC5 and V_{CC} to improve noise performance; otherwise, connect LVCC5 to V_{CC}.
37	37	NO5	T/R Switch 5 Output. When the switch is on, low-voltage signals are passed through from COM5 to NO5, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO5 is limited with clamping diodes on MAX4936/MAX4937.
38	38	LVEE5	Inductor V_{EE} Connection. Connect an inductor between LVEE5 and V_{EE} to improve noise performance; otherwise, connect LVEE5 to V_{EE}.
39	39	LVEE4	Inductor V_{EE} Connection. Connect an inductor between LVEE4 and V_{EE} to improve noise performance; otherwise, connect LVEE4 to V_{EE}.
40	40	NO4	T/R Switch 4 Output. When the switch is on, low-voltage signals are passed through from COM4 to NO4, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO4 is limited with clamping diodes on MAX4936/MAX4937.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX4936/ MAX4938	MAX4937/ MAX4939		
41	41	LVCC4	Inductor V_{CC} Connection. Connect an inductor between LVCC4 and V_{CC} to improve noise performance; otherwise, connect LVCC4 to V_{CC}.
42	42	LVEE3	Inductor V_{EE} Connection. Connect an inductor between LVEE3 and V_{EE} to improve noise performance; otherwise, connect LVEE3 to V_{EE}.
43	43	NO3	T/R Switch 3 Output. When the switch is on, low-voltage signals are passed through from COM3 to NO3, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO3 is limited with clamping diodes on MAX4936/MAX4937.
44	44	LVCC3	Inductor V_{CC} Connection. Connect an inductor between LVCC3 and V_{CC} to improve noise performance; otherwise, connect LVCC3 to V_{CC}.
45	45	LVEE2	Inductor V_{EE} Connection. Connect an inductor between LVEE2 and V_{EE} to improve noise performance; otherwise, connect LVEE2 to V_{EE}.
46	46	NO2	T/R Switch 2 Output. When the switch is on, low-voltage signals are passed through from COM2 to NO2, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO2 is limited with clamping diodes on MAX4936/MAX4937.
47	47	LVCC2	Inductor V_{CC} Connection. Connect an inductor between LVCC2 and V_{CC} to improve noise performance; otherwise, connect LVCC2 to V_{CC}.
48	48	LVEE1	Inductor V_{EE} Connection. Connect an inductor between LVEE1 and V_{EE} to improve noise performance; otherwise, connect LVEE1 to V_{EE}.
49	49	NO1	T/R Switch 1 Output. When the switch is on, low-voltage signals are passed through from COM1 to NO1, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked. NO1 is limited with clamping diodes on MAX4936/MAX4937.
50	50	LVCC1	Inductor V_{CC} Connection. Connect an inductor between LVCC1 and V_{CC} to improve noise performance; otherwise, connect LVCC1 to V_{CC}.
51	51	$\overline{LE}$	Active-Low Latch-Enable Input. Drive $\overline{LE}$ low to change the contents of the latch and update the state of the switches. Drive $\overline{LE}$ high to hold the contents of the latch.
52	52	CLR	Active-High Latch-Clear Input. Drive CLR high to clear the contents of the latch and disable all the switches. When CLR is driven high, the device enters shutdown mode. CLR does not affect the contents of the register.
55	55	COM1	T/R Switch 1 Input. When the switch is on, low-voltage signals are passed through from COM1 to NO1, while high-voltage signals are blocked. When the switch is off, both low-voltage and high-voltage signals are blocked.
56	—	HV1	T/R Switch 1 Input. COM1 follows HV1 when high-voltage signals are present on HV1. HV1 is isolated from COM1 when low-voltage signals are present on COM1.
—	—	EP	Exposed Pad. Internally connected to GND. Connect EP to a large ground plane to maximize thermal performance. Do not use EP as the only GND connection.

Functional Diagram



Detailed Description

The MAX4936–MAX4939 are octal, high-voltage transmit/receive (T/R) switches. The T/R switches are based on a diode bridge topology, and the amount of current in the diode bridges can be programmed through an SPI interface. All devices feature a latch-clear input to asynchronously turn off all T/R switches and put the device into a low-power shutdown mode. The MAX4936/MAX4938 include the T/R switch and grass-clipping diodes, performing both transmit and receive operations. The MAX4937/MAX4939 include just the T/R switch and perform the receive operation only.

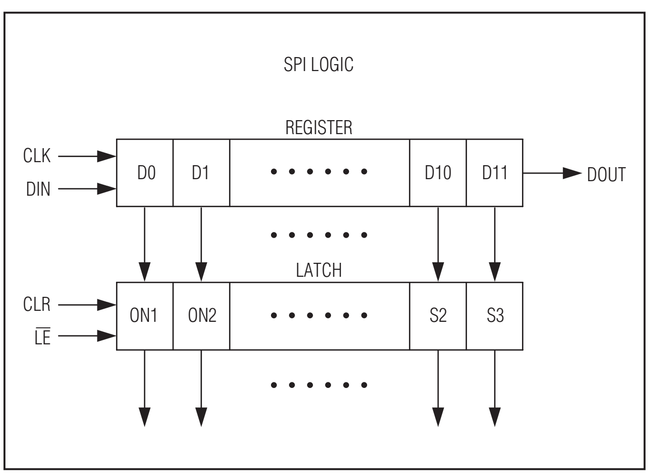


Figure 2. SPI Logic

The MAX4936/MAX4938 transmit path is low impedance during high-voltage transmit and high impedance during low-voltage receive, providing isolation between transmit and receive circuitry. The high-voltage transmit path is high bandwidth, low distortion, and low jitter.

The receive path for all devices is low impedance during low-voltage receive and high impedance during high-voltage transmit, providing protection to the receive circuitry. The low-voltage receive path is high bandwidth, low noise, low distortion, and low jitter. Each T/R switch can be individually programmed on or off, allowing these devices to also be used as receive path multiplexers.

The MAX4936/MAX4937 feature clamping diodes to protect the receiver input from voltage spikes due to leakage currents flowing through the T/R switches during transmission. The MAX4938/MAX4939 do not have clamping diodes and rely on clamping diodes integrated in the receiver front-end.

Serial Interface

All the devices are controlled by a serial interface with a 12-bit serial shift register and transparent latch (Figure 2). Each of the first 4 data bits controls the bias current into the diode bridges (see Figure 3 and Table 2), while the remaining 8 data bits control a T/R switch (Table 1). Data on DIN is clocked with the most significant bit (MSB) first into the shift register on the rising edge of CLK. Data is clocked out of the shift register onto DOUT on the rising edge of CLK. DOUT reflects the status of DIN, delayed by 12 clock cycles (Figure 4).

Transmit/Receive Switch

The T/R switch is based on a diode bridge topology. The amount of bias current into each diode bridge is adjustable by setting the S0–S3 switches through the serial interface (see Figure 3 and Table 2).

Latch Enable ($\overline{LE}$)

Drive $\overline{LE}$ logic-low to change the contents of the latch and update the state of the T/R switches (Figure 4). Drive $\overline{LE}$ logic-high to hold the contents of the latch and prevent changes to the switches' states. To reduce noise due to clock feedthrough, drive $\overline{LE}$ logic-high while data is clocked into the shift register. After the data shift register is loaded with valid data, pulse $\overline{LE}$ logic-low to load the contents of the shift register into the latch.

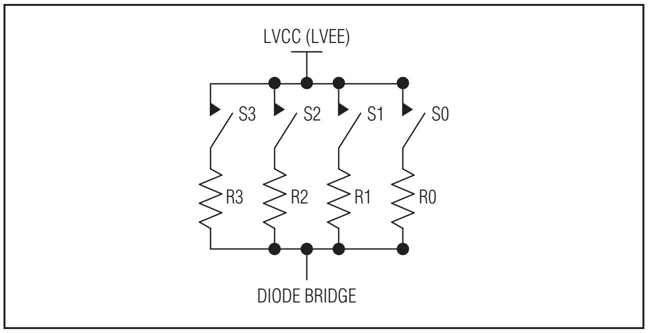


Figure 3. Diode Bias Current Control

Latch Clear (CLR)

Drive CLR logic-high to reset the contents of the latch to zero and open all T/R switches. CLR does not affect the contents of the shift register. Once CLR is high again, and $\overline{LE}$ is driven low, the contents of the shift register are loaded into the latch.

Power-On Reset

The devices feature a power-on-reset circuit to ensure all switches are off at power-on. The internal 12-bit serial shift register and latch are set to zero on power-up.

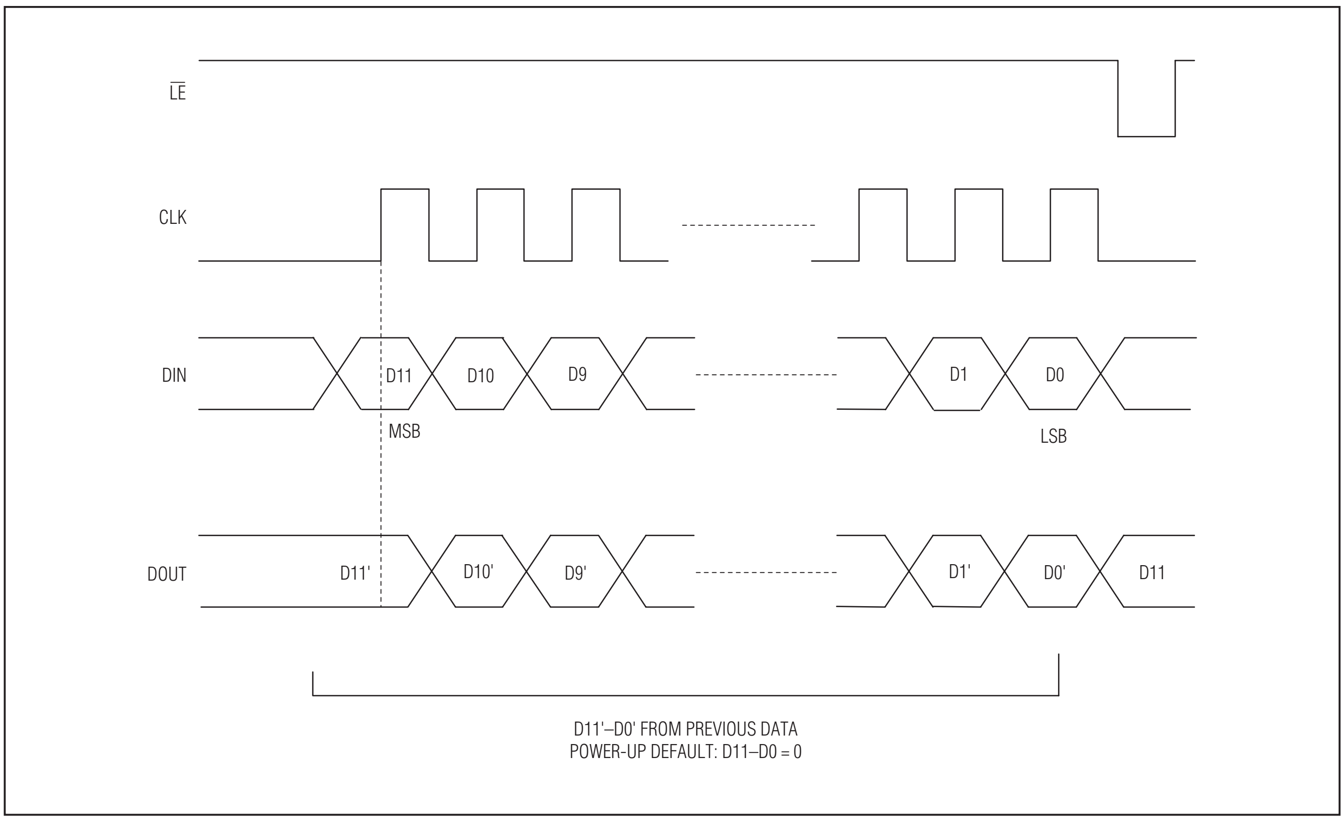


Figure 4. Latch-Enable Interface Timing

Table 1. Serial Interface Programming

DATA BITS												CONTROL BITS		FUNCTION											
D0 (LSB)	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11 (MSB)	$\overline{LE}$	CLR	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	S0	S1	S2	S3
L												L	L	Off											
H												L	L	On											
	L											L	L		Off										
	H											L	L		On										
		L										L	L			Off									
		H										L	L			On									
			L									L	L				Off								
			H									L	L				On								
				L								L	L					Off							
				H								L	L					On							
					L							L	L						Off						
					H							L	L						On						
						L						L	L							Off					
						H						L	L							On					
							L					L	L								Off				
							H					L	L								On				
								L				L	L									Off			
								H				L	L									On			
									L			L	L										Off		
									H			L	L										On		
										L		L	L											Off	
										H		L	L											On	
											L	L	L												Off
											H	L	L												On
X	X	X	X	X	X	X	X	X	X	X	X	H	L	Hold Previous State											
X	X	X	X	X	X	X	X	X	X	X	X	X	H	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off

L = Low, H = High, X = Don't care.

Table 2. Diode Bias Current

SWITCHES				RESISTORS (Ω)				RESISTOR COMBINATION	TYPICAL DIODE BRIDGE CURRENT (mA) vs. S[3:0] CONTROL BITS (*)	
S3	S2	S1	S0	R3	R2	R1	R0	(Ω)	V_{CC} = 3.0V	V_{CC} = 5.0V
0	0	0	0	350	700	1400	2800	—	0	0
0	0	0	1	350	700	1400	2800	2800	0.78	1.50
0	0	1	0	350	700	1400	2800	1400	1.58	3.00
0	0	1	1	350	700	1400	2800	933	2.36	4.50
0	1	0	0	350	700	1400	2800	700	3.14	6.00
0	1	0	1	350	700	1400	2800	560	3.98	7.50
0	1	1	0	350	700	1400	2800	467	4.72	9.00
0	1	1	1	350	700	1400	2800	400	5.50	10.50
1	0	0	0	350	700	1400	2800	350	6.28	12.00
1	0	0	1	350	700	1400	2800	311	7.08	13.50
1	0	1	0	350	700	1400	2800	280	7.86	15.00
1	0	1	1	350	700	1400	2800	255	8.64	16.50
1	1	0	0	350	700	1400	2800	233	9.42	18.00
1	1	0	1	350	700	1400	2800	215	10.22	19.50
1	1	1	0	350	700	1400	2800	200	11.00	21.00
1	1	1	1	350	700	1400	2800	187	11.78	22.50

*V_{EE} = -V_{CC}

Octal High-Voltage Transmit/Receive Switches

Applications Information

For medical ultrasound applications, see Figures 5, 6, and 7.

Ultrasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, F1 represents reflections from tissue and F2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude, and hence the measurement is defined with one input tone 25dB lower than the other. The IMD3 product of interest (F1 - (F2 - F1)) presents itself as an undesired Doppler error signal in ultrasound applications. See Figure 8.

Logic Levels

The digital interface inputs CLK, DIN, $\overline{LE}$, and CLR are tolerant of up to +5.5V, independent of the V_{DD} supply voltage, allowing compatibility with higher voltage controllers.

Daisy-Chaining Multiple Devices

Digital output DOUT is provided to allow the connection of multiple devices by daisy-chaining (Figure 9). Connect each DOUT to the DIN of the subsequent device in the chain. Connect CLK, $\overline{LE}$, and CLR inputs of all devices, and drive $\overline{LE}$ logic-low to update all devices simultaneously. Drive CLR high to open all the switches simultaneously. Additional shift registers can be included anywhere in series with the device data chain.

Supply Sequencing and Bypassing

The devices do not require special sequencing of the V_{DD}, V_{CC}, and V_{EE} supply voltages; however, analog switch inputs must be unconnected, or satisfy $V_{EE} \le (V_{HV\_}, V_{COM\_}, V_{NO\_}) \le V_{CC}$ during power up and power down. Bypass V_{DD}, V_{CC}, and V_{EE} to GND with a 1µF ceramic capacitor as close as possible to the device.

PCB Layout

The pin configuration is optimized to facilitate a very compact physical layout of the device and its associated discrete components. A typical application for this device might incorporate several devices in close proximity to handle multiple channels of signal processing.

The exposed pad (EP) of the TQFN-EP package provides a low thermal resistance path to the die. It is important that the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP must be soldered to a ground plane on the PCB, either directly or through an array of plated through holes.

Application Diagrams

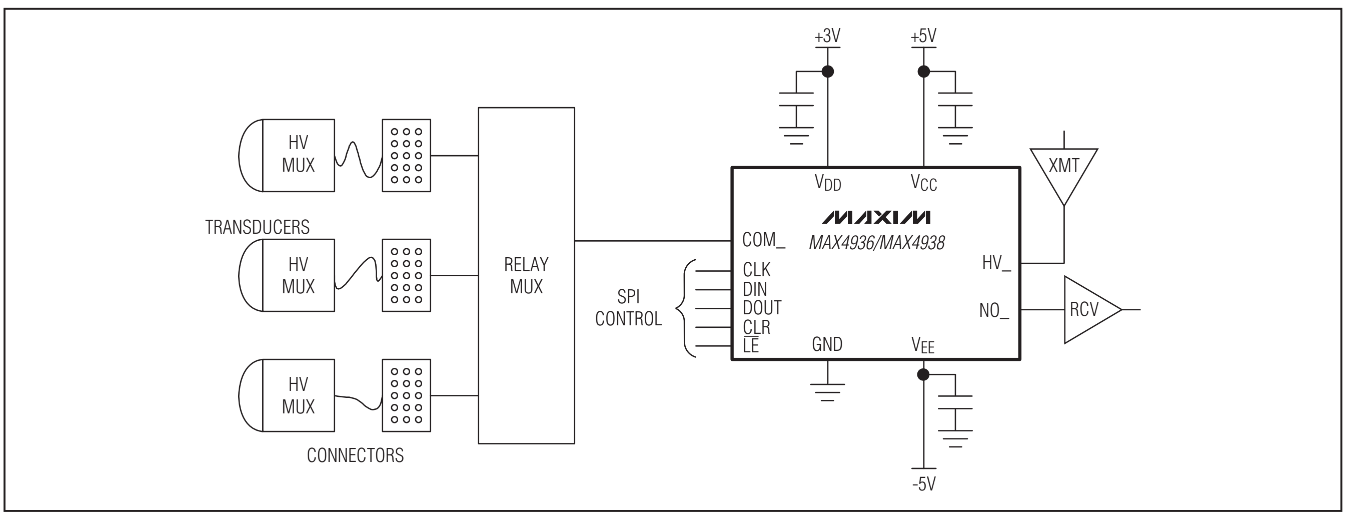


Figure 5. Ultrasound T/R Path with One Transmit per Receive Channel (One Channel Only)

Application Diagrams (continued)

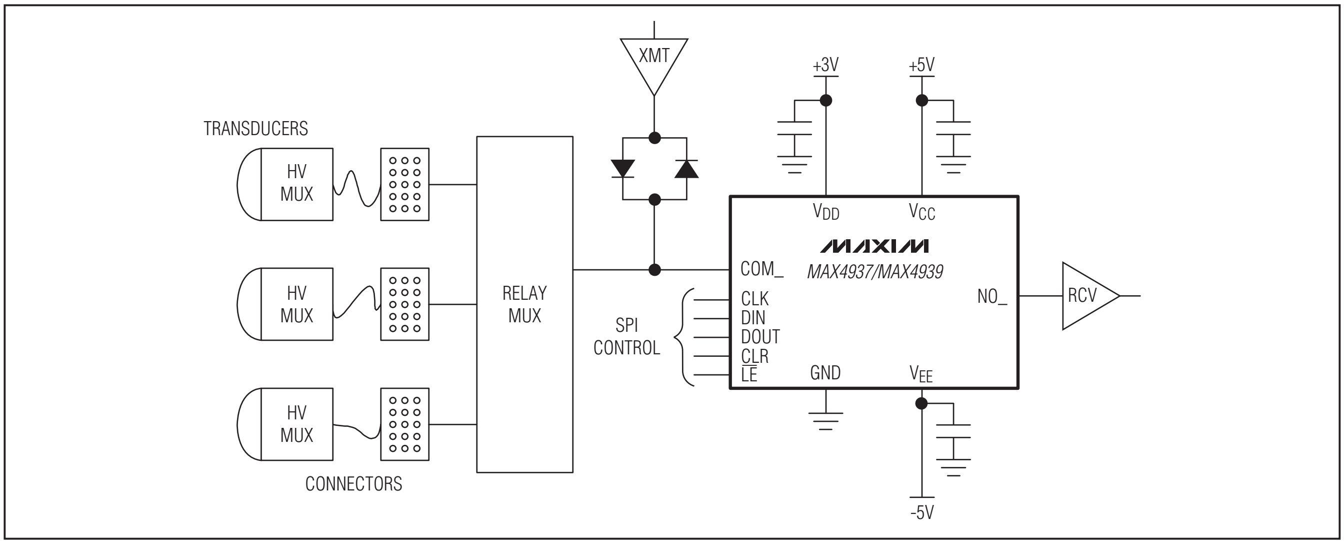


Figure 6. Ultrasound T/R Path with One Transmit per Receive Channel and External Isolation (One Channel Only)

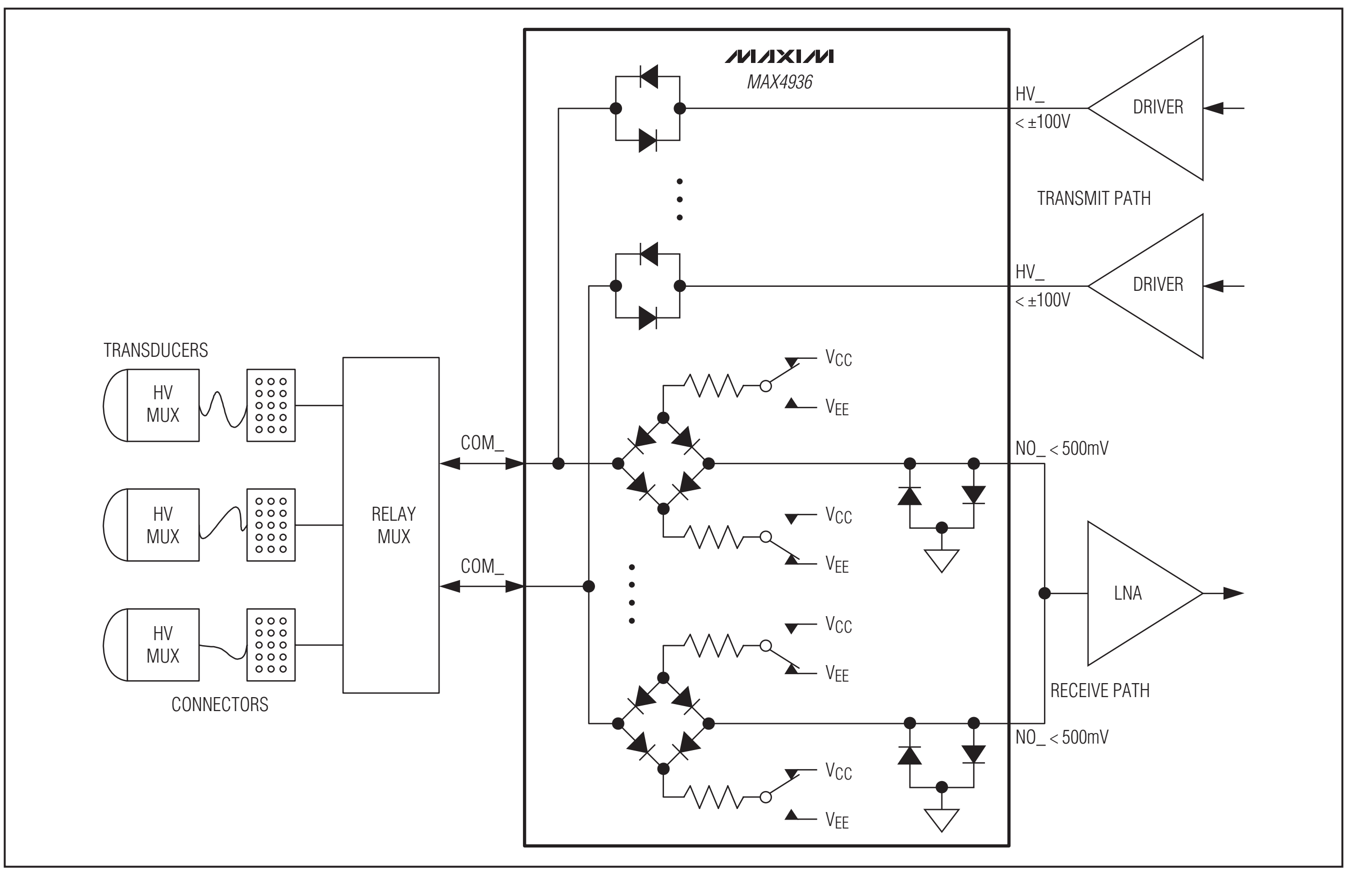


Figure 7. Ultrasound T/R Path with Multiple Transmits per Receive Channel

Octal High-Voltage Transmit/Receive Switches

Application Diagrams (continued)

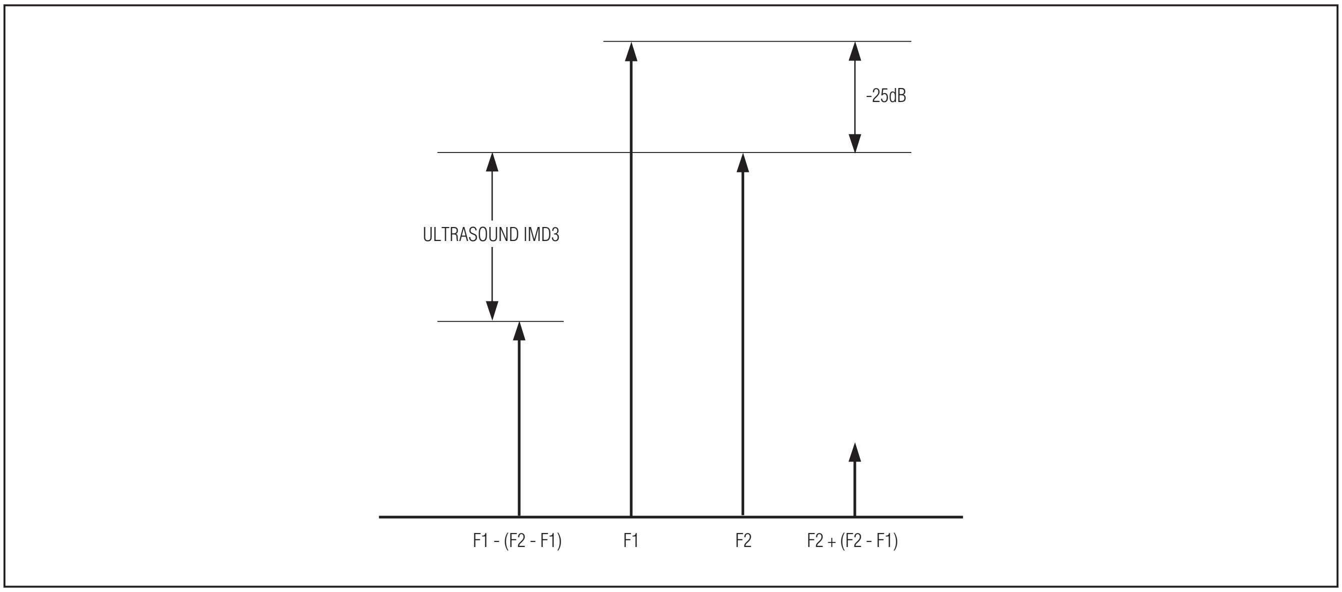


Figure 8. Ultrasound IMD3 Measurement Technique

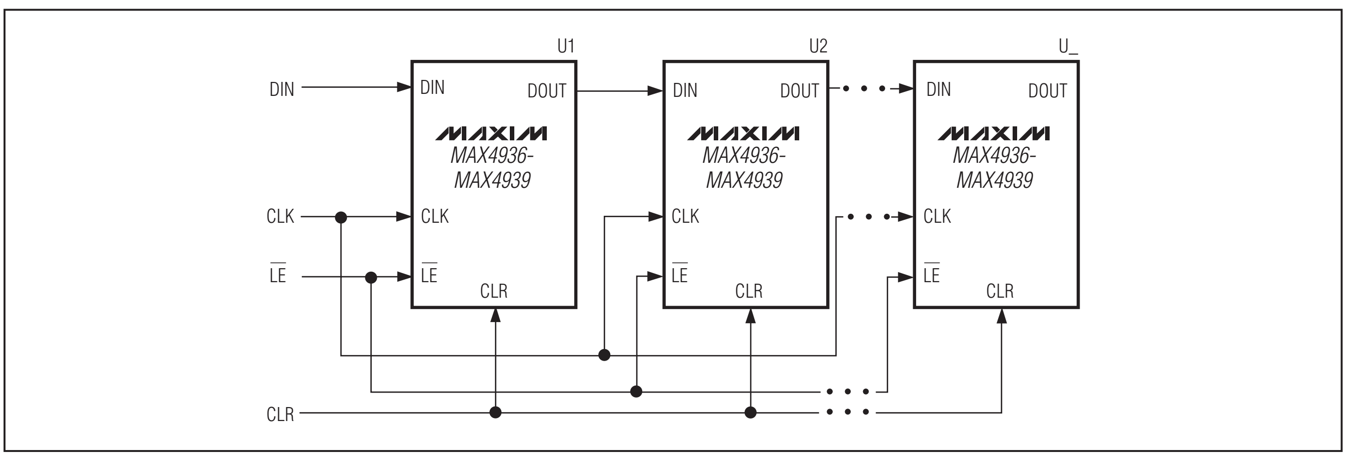


Figure 9. Interfacing Multiple Devices by Daisy-Chaining

Chip Information

PROCESS: BCDMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T56511+1	21-0187	90-0087

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/10	Initial release	—
1	3/11	Updated the Diode Bridge Turn-Off Time and the NO_ On Capacitance in the *Electrical Characteristics*, updated Figure 7	3, 4, 17

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